



# StellarStudio Clocktree Configurator

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# Contents

<b>1 Introduction .....</b>	<b>4</b>
<b>2 Create a ClockTree Wizard configuration .....</b>	<b>5</b>
<b>3 ClockTree Editors .....</b>	<b>10</b>
<b>4 ClockTree wizard quick guide .....</b>	<b>13</b>
4.1 Selectors and dividers .....	13
4.2 Clock tree Reset to default value .....	15
4.3 Clock tree Errors management .....	16
4.4 Clock tree configuration Integration .....	16
<b>5 Disclaimer .....</b>	<b>18</b>

## List of figures

Figure 1. StellarStudio .....	4
Figure 2. Create a project .....	5
Figure 3. Project is created .....	6
Figure 4. Select other .....	6
Figure 5. Select a clock configuration .....	7
Figure 6. Choose a name for the clock configuration file .....	8
Figure 7. Configuration created .....	9
Figure 8. ClockTree tabular editor .....	10
Figure 9. ClockTree graphical editor .....	11
Figure 10. opening textual editor .....	12
Figure 11. opening graphical editor (click on editor first) .....	12
Figure 12. Clocktree elements (graphical view) .....	13
Figure 13. Clocktree elements (tabular view) .....	14
Figure 14. Graphical selector .....	15
Figure 15. Tabular selector .....	15
Figure 16. Clock tree image reset to default value .....	15
Figure 17. Clock tree image error display .....	16
Figure 18. Clock tabular editor error display .....	16
Figure 19. Clock tree generated C header configuration .....	17
Figure 20. Update C includes .....	17

# 1 Introduction

Figure 1: StellarStudio



The ClockTree wizard is an intuitive end user graphical assistant dedicated to clock system configuration.

The configuration is dynamically checked against the microcontroller possible options.

The user configuration is synchronized with the StellarStudio application.

## 2 Create a ClockTree Wizard configuration

You can create as many configurations as needed for a given device.

Each configuration file is suffixed with <device\_name>\_clk (for example .Sr5e1\_clk)

### Creating a project

Configuration files are stored in general development projects.

To create a development project:

1/ Select File -> New -> Project-> General -> Project

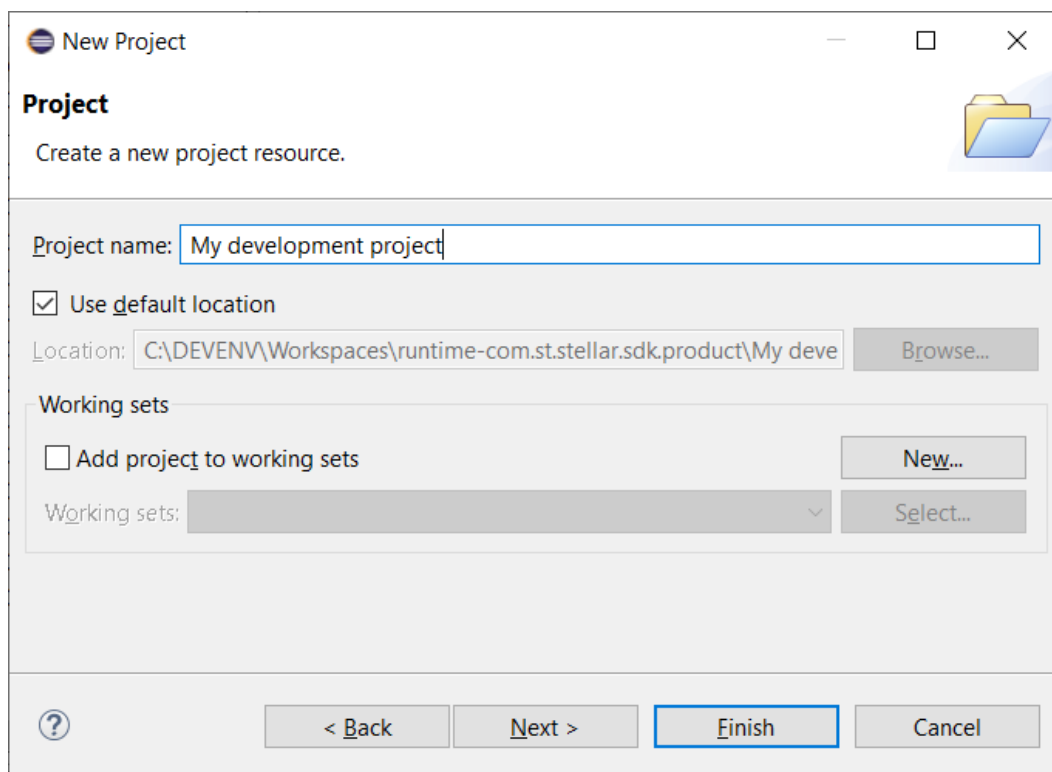
2/ Click "Next"

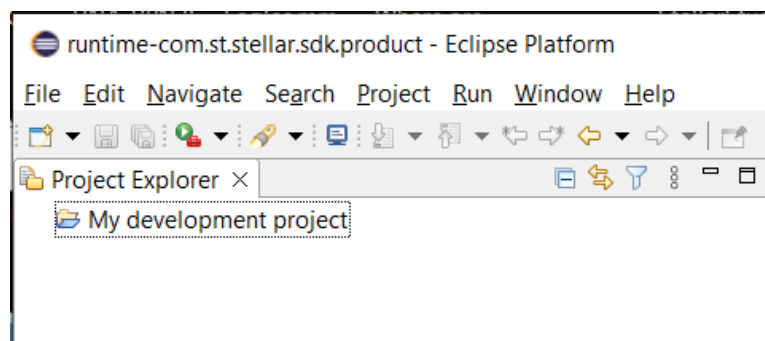
3/ Name your project

4/ Click "Finish"

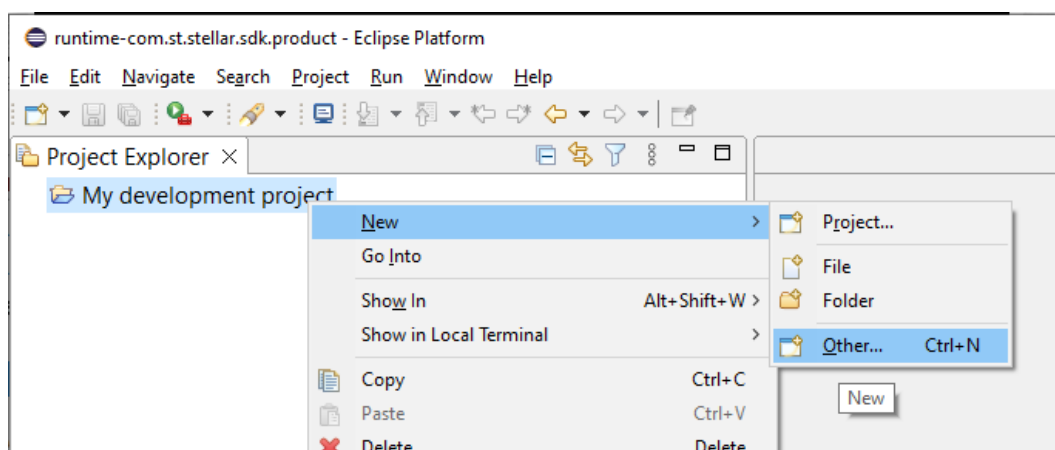
Your project is created and appears in the project explorer

**Figure 2: Create a project**



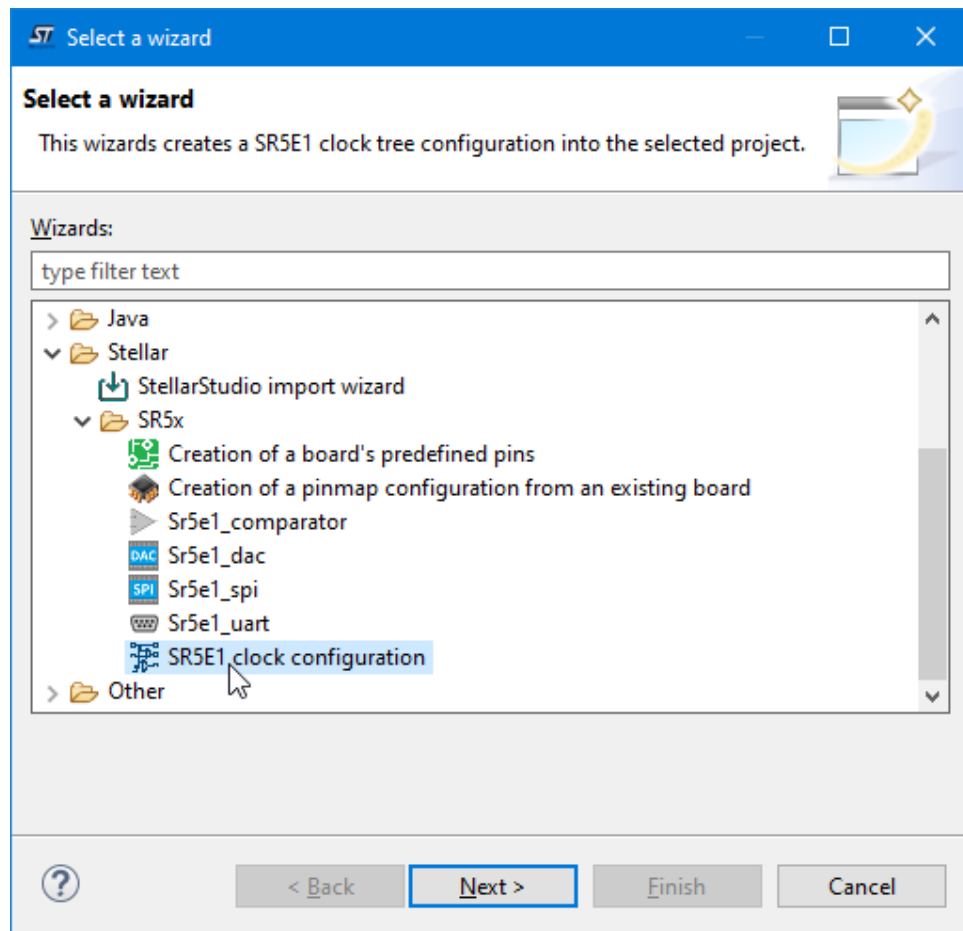
**Figure 3: Project is created****Create a clocktree configuration file**

- 1/ Select your development project
- 2/ Right click and select New->Other

**Figure 4: Select other**

- 3/ Select in the wizard a device clock configuration

Figure 5: Select a clock configuration



4/ Click "Next"

5/ Provide a name to your configuration

**BEWARE NOT TO MODIFY THE SUFFIX !!!! (eg: Sr5e1\_clk)**

Figure 6: Choose a name for the clock configuration file

**Creation of a clocktree configuration**

**Clock configuration**  
Create a SR5E1 clock configuration model

Enter or select the parent folder:

My development project

My development project

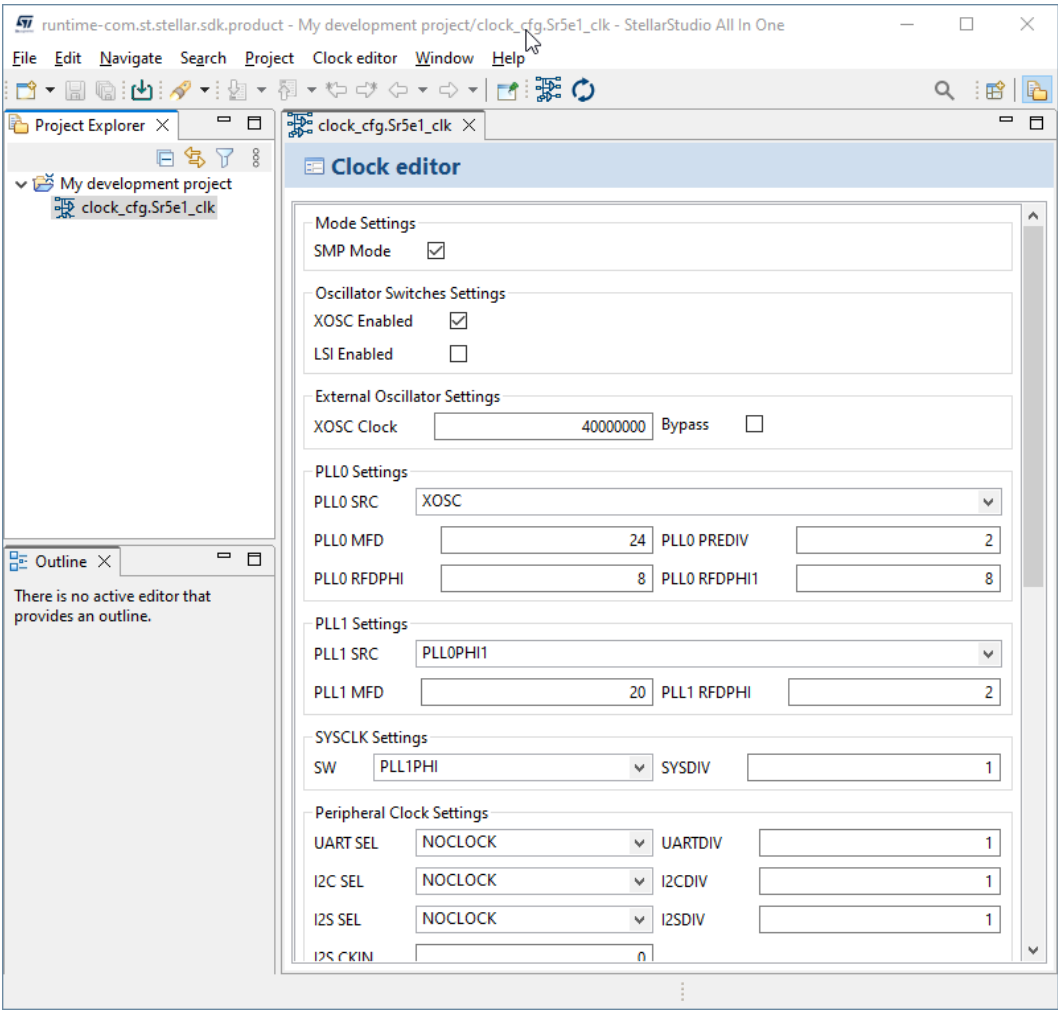
File name: clock\_cfg.Sr5e1\_clk

Advanced >>

? < Back Next > Finish Cancel



Figure 7: Configuration created



### 3 ClockTree Editors

There are two Clocktree editors associated with cloctree configurations.

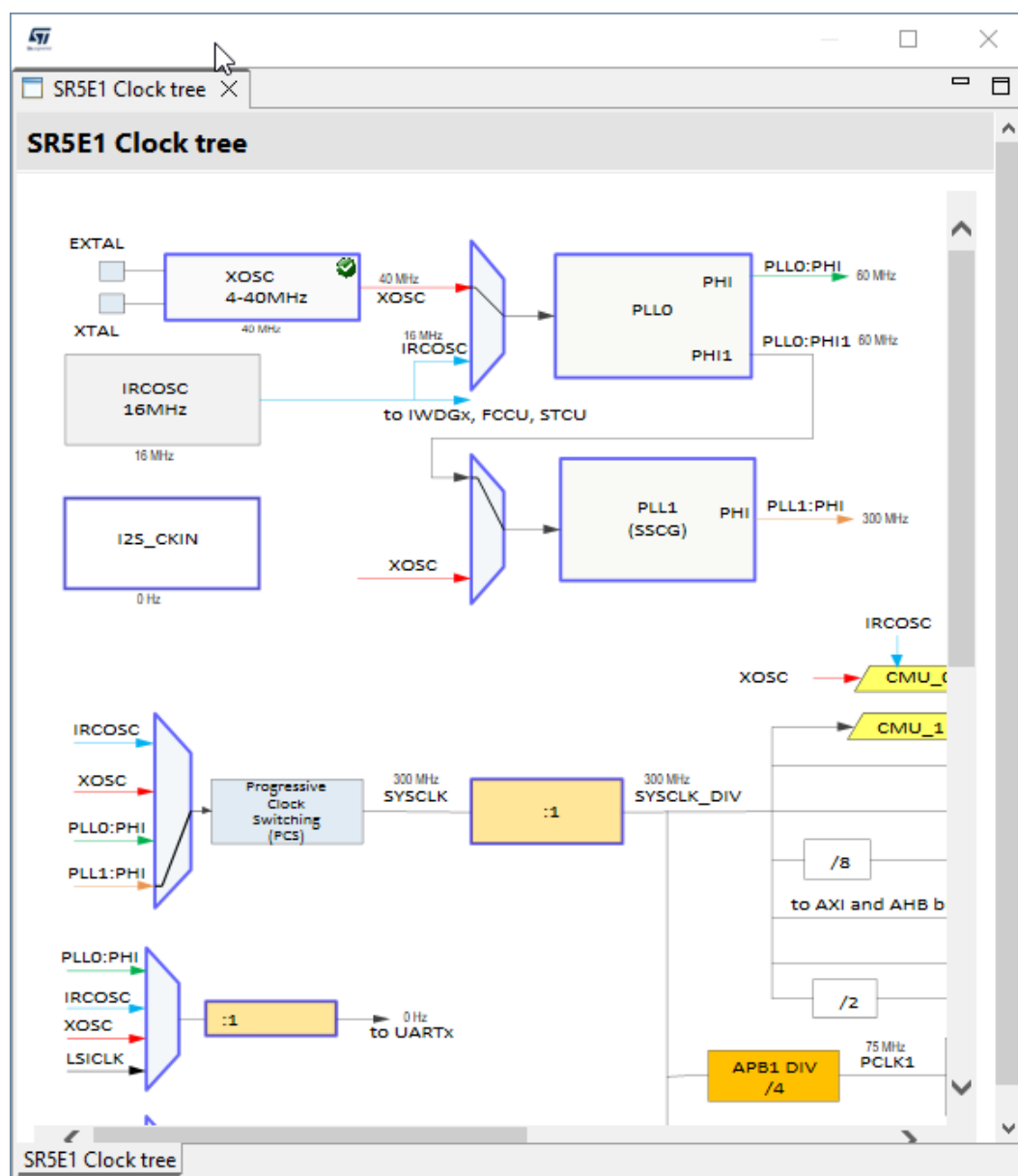
- \* Tabular editor
- \* Graphical editor

**Figure 8: ClockTree tabular editor**

The screenshot shows the 'Clock editor' window with the following settings:

- Mode Settings**
  - SMP Mode: ☒
- Oscillator Switches Settings**
  - XOSC Enabled: ☒
  - LSI Enabled: ☐
- External Oscillator Settings**
  - XOSC Clock: 40000000 Bypass ☐
- PLL0 Settings**
  - PLL0 SRC: XOSC
  - PLL0 MFD: 24 PLL0 PREDIV: 2
  - PLL0 RFDPHI: 8 PLL0 RFDPHI1: 8
- PLL1 Settings**
  - PLL1 SRC: PLL0PHI1
  - PLL1 MFD: 20 PLL1 RFDPHI: 2
- SYSCLK Settings**
  - SW: PLL1PHI SYSDIV: 1
- Peripheral Clock Settings**
  - UART SEL: NOCLOCK UARTDIV: 1
  - I2C SEL: NOCLOCK I2CDIV: 1
  - I2S SEL: NOCLOCK I2SDIV: 1

Figure 9: ClockTree graphical editor



### Opening editors

The tabular editor is the default edit mode. It is open by double clicking on the configuration file

The graphical editor is opened by single clicking on the associated icon

Figure 10: opening textual editor

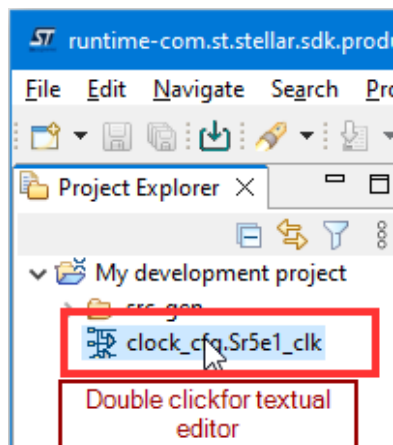
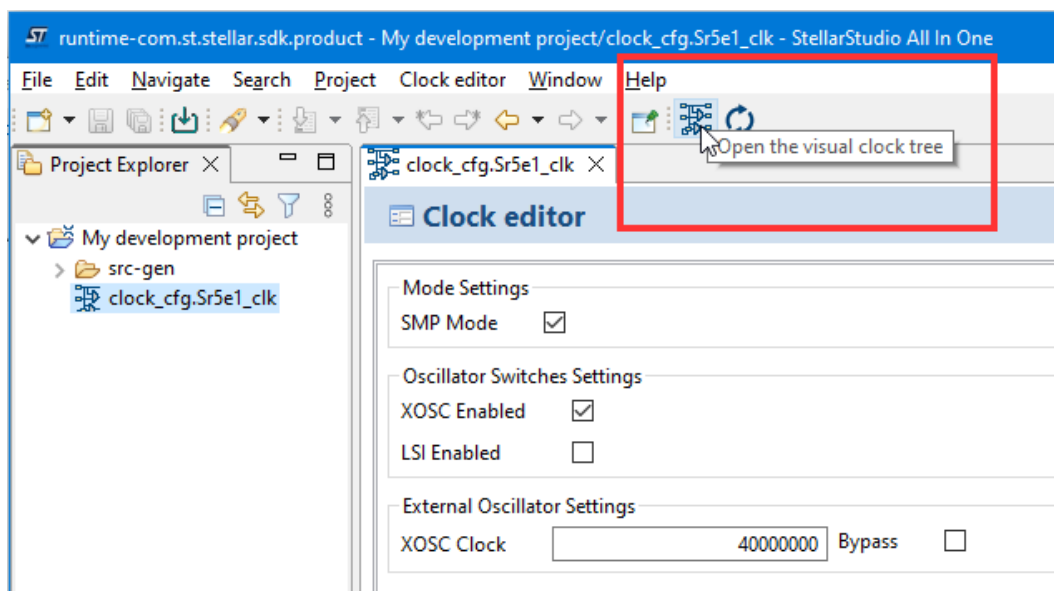


Figure 11: opening graphical editor (click on editor first)



## 4 ClockTree wizard quick guide

The scope of the Clocktree configurator is to simplify the clock system configuration.

Input clocks are used to produce the expected clocks (clock points) that can be used by the various IPs

The clock points are computed based on the user selection done in the editors (tabular or graphical)

The changes in the editors are synchronized.

There are two basic kind of operations that can be done : Selectors and dividers

### 4.1 Selectors and dividers

Selectors are used to define a clock path in the clock tree.

Dividers are used to lower input frequencies.

The value of these clock points is the result of the various operations done by the selectors and the dividers in a clock path.

Clock points are located at the output of clock paths .

**Figure 12: Clocktree elements (graphical view)**

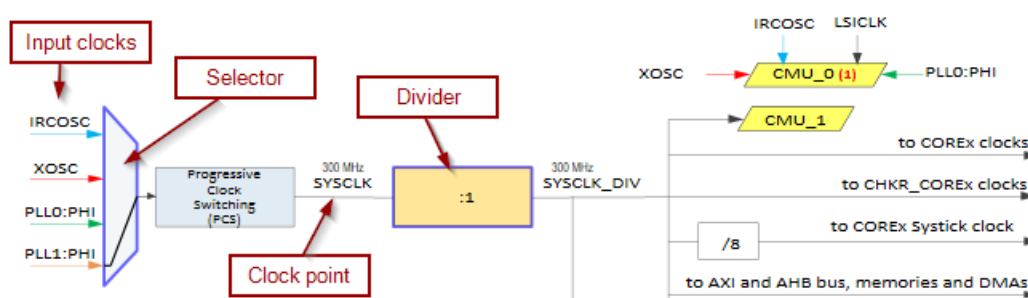


Figure 13: Clocktree elements (tabular view)

The screenshot shows the 'Clock editor' window with the following settings:

Section	Parameter	Value
PLL1 MFD	PLL1 MFD	20
	PLL1 RFDPHI	2
SYSCLK Settings	SW	PLL1PHI
	SYSDIV	1
Peripheral Clock Settings	UART SEL	NOCLOCK
	UARTDIV	1
	I2C SEL	NOCLOCK
	I2CDIV	1
	I2S SEL	NOCLOCK
	I2SDIV	1
	I2S CKIN	0
	FDCAN SEL	NOCLOCK
	FDCANDIV	1
	ADC SEL	NOCLOCK
ADCDIV	1	
SDADC SEL	NOCLOCK	
SDADC DIV	1	
MCO SEL	NOCLOCK	
MCODIV	1	
RTC SEL	NOCLOCK	
LSIDIV	1	
System Clock Points	XOSC	40000000
	IRCO SC	16000000
	LSI	0
	SYSCLK	300000000
	PCLK1	75000000
	PCLK2	150000000
	PLL0IN	40000000
	PLL0PFD	20000000
PLL0VCO	960000000	
PLL0PHI	60000000	
PLL0PHI1	60000000	
PLL1IN	60000000	

### Selectors

Selectors are modified by selection and left click in both modes (graphical and tabular)

Figure 14: Graphical selector

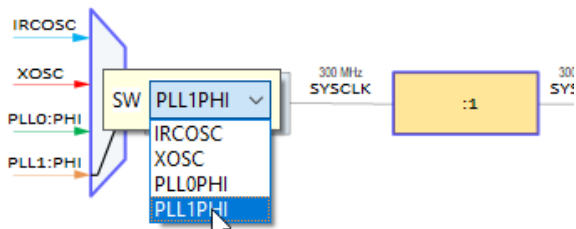


Figure 15: Tabular selector

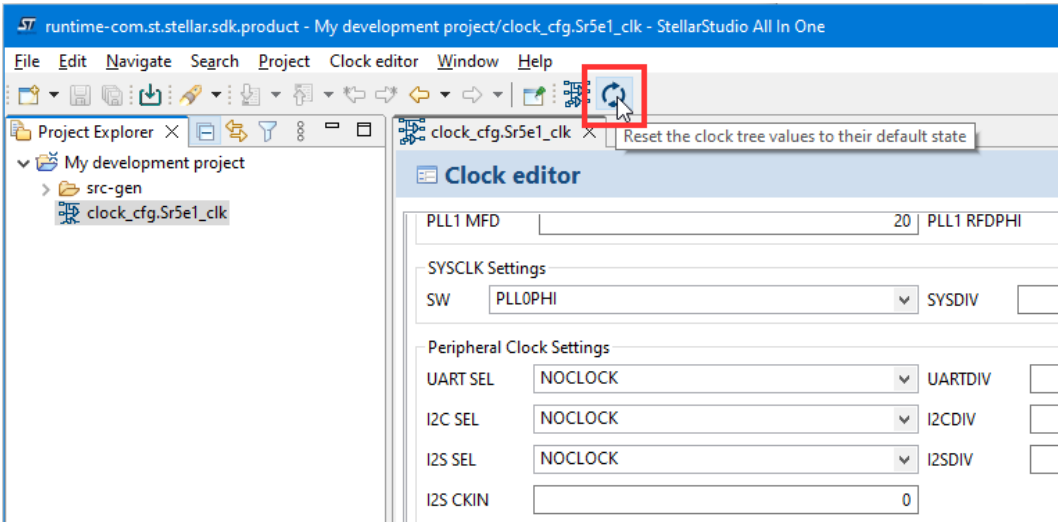
SYSCLK Settings	
SW	PLL0PHI
Peripheral Clock Settings	
UART SEL	NOLOCK
I2C SEL	NOLOCK
I2S SEL	NOLOCK

4.2 Clock tree Reset to default value

Reset clock tree values

Clicking on the icon can reset clock tree values to their default value state.

Figure 16: Clock tree image reset to default value



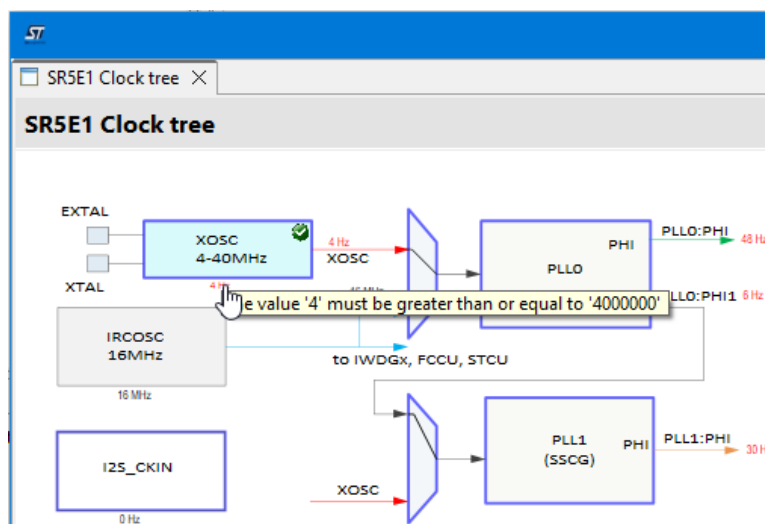
## 4.3 Clock tree Errors management

### Errors visualization

Errors are displayed in RED color in the image and in the tabular editor.

A mouse over the red section indicates the nature of the error.

**Figure 17: Clock tree image error display**



**Figure 18: Clock tabular editor error display**

System Clock Points	
XOSC	4
IRCOSC	16000000
LSI	0

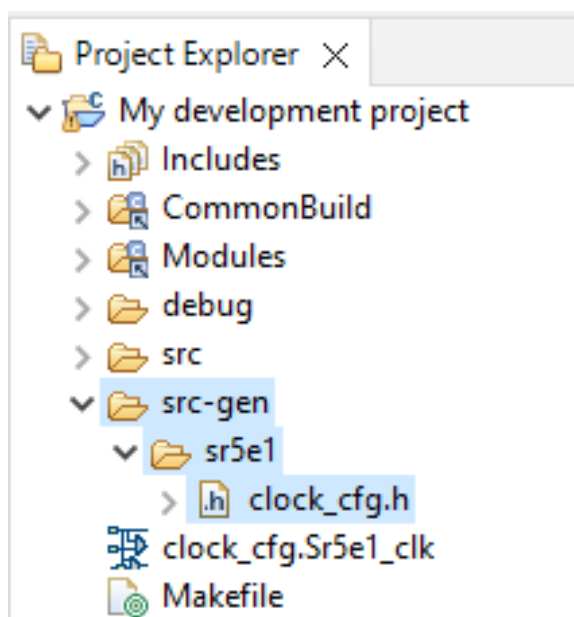
## 4.4 Clock tree configuration Integration

### generated C header and location

the generated C header is located according to the device name.



Figure 19: Clock tree generated C header configuration



### Makefile adaptation

the Makefile must be adapted to include the device folder.

Figure 20: Update C includes

```
# C includes
#####
# PLEASE UPDATE IT FOR GENERATED CODE
# DO NOT FORGET TO CLEAN THE PROJECT
# FOR THE DEPENDENCIES FILES
#####
C_INCLUDES += \
    src-gen/ \
    src-gen/${CONFIG_DEVICE}
```

### Compilation with new Clock tree configuration

it just needs to Clean and Build again the project.

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